Amendments to the Specification

Please replace the paragraph beginning at page 12, line 29, with the following rewritten paragraph:

FIG. 6 graphically illustrates the timing of an exemplary asymmetric data path. In accordance with an exemplary embodiment of the present invention, input data 502 is represented by data bits D1, D2, D3, etc. and includes 32 data bits in a preferred embodiment. The wave/timing diagram in FIG. 6 shows the timing perspective of how 32 bit-wide input data 502 is converted to 64 bit-wide output data 512. In accordance with an exemplary embodiment of the present invention a first gate element 302 samples the input data 316 (502) on the "rising" edge of the clock signal 314 (506) ~~(504)~~. In addition, a second gate element 304 samples the input data 316 (502) on the "falling" edge of the clock signal 314 (508) ~~(504)~~. In the described exemplary embodiment, the master gate 306 (510) converts the two 32 bit-wide data streams 506 ~~502~~ and 508 ~~504~~ to a 64 bit wide parallel data stream using a subsequent rising edge of the clock signal 504. In addition, the 64 bit-wide output data with CRC appended is also illustrated.

Please replace the paragraph beginning at page 12, line 29, with the following rewritten paragraph:

In the described exemplary embodiment, MACs 104(a) and 104(b) perform flow independent MAC layer operations on the inbound packets. For example, MACs 104(a) and 104(b) may process the received Ethernet packets and forward higher layer packets to the ~~PCS~~ PSC 102. The ~~PCS~~ PSC 102 preferably receives the inbound packets, classifies the packets, generates application data for the inbound packets, modifies the inbound packets in accordance

with the application data, and transmits the modified inbound packets onto, for example, a switching backplane.